AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) A method for modeling a physical memory for use in an electronic circuit design, the method comprising ~~the steps of~~:

~~modeling a memory write operation of the electronic circuit design using a lookup table;~~

~~modeling a memory read operation of the electronic circuit design using the lookup table; and~~

accessing a description of the electronic circuit design;

replacing a portion of [[a]] the description of the electronic circuit design with ~~the~~ a lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical ~~memory.~~ memory, the lookup table including a total number of entries greater than or equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by computing a total number of memory operations that can be performed per clock cycle and multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles; and

simulating the electronic circuit design using the description, wherein simulating includes modeling a memory write operation of the electronic circuit design using the lookup table and modeling a memory read operation of the electronic circuit design using the lookup table.

2. (currently amended) The method of claim 1, wherein ~~the step of~~ modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic circuit design;

receiving the plurality of write data bits corresponding to write data written to the physical memory at the write address; and

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted.

3. (currently amended) The method of claim 2, wherein ~~the step of~~ modeling a memory

write operation further comprises the step of:

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and a valid bit of the first entry is asserted.

4. (currently amended) The method of claim 2, wherein ~~the step of~~ modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

5. (currently amended) The method of claim 1, wherein ~~the step of~~ modeling a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design; and

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted.

6. (currently amended) The method of claim 5, wherein ~~the step of~~ modeling a memory read operation further comprises the step of:

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and a valid bit of the first entry is asserted.

7. (currently amended) The method of claim 5, wherein ~~the step of~~ modeling a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary data value to a data field of the

second entry;

asserting the valid bit of the second entry; and

returning the arbitrary data value.

8. (original) The method of claim 7, wherein the arbitrary data value represents an initial value of the plurality of read data bits after an initialization step.

9. (cancelled)

10. (currently amended) The method of ~~claim 9~~ claim 1, further comprising ~~the steps of~~:

determining a number of memory read operations in a property; and

adding the number of memory read operations in a property to the total number of memory operations that can occur over the given number of clock cycles.

11. (original) The method of claim 1, further comprising the step of:

initializing a plurality of bits in a data field of an entry of the lookup table to an initial value.

12. (currently amended) A method for modeling an uninterpreted combinational block of an electronic circuit design in a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the method comprising ~~the steps of~~:

~~initializing the lookup table;~~

~~receiving the argument;~~

~~determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted;~~

~~returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument; and~~

accessing a description of the electronic circuit design;

replacing a portion of [[a]] the description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combinational block, and wherein the lookup table in the description represents the uninterpreted combinational ~~block.~~ block, the lookup table

including a total number of entries greater than or equal to a total number of times the uninterpreted combinational block will be evaluated over a given number of clock cycles, the total number of times the uninterpreted combinational block will be evaluated being computed by computing a total number of times the uninterpreted combinational block will be evaluated per clock cycle and multiplying the total number of times the uninterpreted combinational block will be evaluated per clock cycle by the given number of clock cycles; and

simulating the electronic circuit design using the description, wherein simulating includes:

initializing the lookup table,

receiving the argument,

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted, and

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.

13. (currently amended) The method of claim 12, further comprising ~~the steps of~~ writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.

14. (currently amended) A method for modeling a physical memory in an electronic circuit design, the method comprising ~~the steps of~~:

~~receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;~~

~~receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;~~

~~modeling a memory write operation of the electronic circuit design in a memory model to represent a memory write operation in the physical memory;~~

~~determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted;~~

accessing a description of the electronic circuit design;

replacing a portion of [[a]] the description of the electronic circuit design with ~~the~~ a memory model, wherein the portion of the electronic circuit design relates to the physical memory, and wherein the memory model in the description represents the physical ~~memory.~~ memory, the memory model including a total number of entries that is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by:

determining a number of read ports of the physical memory,

determining a number of write ports of the physical memory,

computing a total number of memory operations that can be performed per clock cycle based on the number of read ports and write ports, and

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles; and

simulating the electronic circuit design using the description, wherein simulating includes:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits,

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address,

modeling a memory write operation of the electronic circuit design in the memory model to represent a memory write operation in the physical memory, and

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted.

15. (original) The method of claim 14, wherein the plurality of write data bits are written to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

16. (original) The method of claim 14, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

17. (currently amended) The method of claim 14, further comprising ~~the steps of~~:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;

modeling a memory read operation in the memory model to represent a memory read operation in the physical memory; and

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.

18. (original) The method of claim 17, wherein the plurality of read data bits from a data field of the entry is returned if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.

19. (original) The method of claim 17, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

20. (original) The method of claim 14, wherein the memory model comprises a lookup table.

21. (cancelled)

22. (currently amended) The method of ~~claim 21~~ claim 14, further comprising ~~the steps of~~:

determining a number of memory read operations in a property; and

adding the number of memory read operations in a property to the total number of memory operations that can occur over the given number of clock cycles.

23. (currently amended) A method for modeling an electronic circuit design having a physical memory, the physical memory being represented by a lookup table, the method comprising ~~the steps of~~:

~~creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit;~~

creating a hardware description language description of ~~the lookup table and~~ a plurality of components of the electronic circuit design including the physical memory~~, wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design~~;

synthesizing a gate level description of ~~the lookup table and~~ the plurality of components of the electronic circuit design including the physical memory;

replacing a portion of the gate level description relating to the physical memory with the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by:

determining a total number of memory read ports in the physical memory,

determining a total number of memory write ports in the physical memory,

computing a total number of memory operations that can be performed per clock cycle based on the number of read ports and write ports, and

multiplying the total number of memory operations that can be performed per clock cycle

with the given number of clock cycles; and

verifying operation of the electronic circuit design using a set of properties.

24. (currently amended) The method of claim 23, ~~wherein the step of creating the lookup table comprises the steps of~~ further comprising modeling at least one memory operation of the electronic circuit design by:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;

determining whether the lookup table comprises an entry that contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted;

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and a valid bit of the entry is asserted;

determining whether the lookup table comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and

writing the plurality of write data bits to the data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

25. (original) The method of claim 24, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

26. (original) The method of claim 24, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

27. (cancelled)

28. (currently amended) The method of ~~claim 27~~ claim 23, further comprising the steps of:

determining a number of memory read operations performed in the set of properties; and

adding the number of memory read operations performed in the set of properties to the total number of memory operations that can occur over the given number of clock cycles.

29. (currently amended) A processor readable storage medium having processor readable code embodied on the processor readable storage medium, the processor readable code for programming a processor to perform a method for creating a memory model for use in modeling an electronic circuit design having a physical memory, the method comprising ~~the steps of~~:

~~modeling a memory write operation of the electronic circuit design using a lookup table;~~

~~modeling a memory read operation of the electronic circuit design using the lookup table; and~~

accessing a description of the electronic circuit design;

replacing a portion of [[a]] the description of the electronic circuit design with [[the]] a lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical ~~memory.~~ memory, the lookup table including a total number of entries greater than or equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by computing a total number of memory operations that can be performed per clock cycle and multiplying the total number of memory

operations that can be performed per clock cycle by the given number of clock cycles; and

simulating the electronic circuit design using the description, wherein simulating includes modeling a memory write operation of the electronic circuit design using the lookup table and modeling a memory read operation of the electronic circuit design using the lookup table.

30. (currently amended) The processor readable storage medium of claim 29, wherein ~~the step of~~ modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;

receiving the plurality of write data bits written to the physical memory at the write address;

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted; and

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and the valid bit of the first entry is asserted.

31. (currently amended) The processor readable storage medium of claim 30, wherein ~~the step of~~ modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

32. (currently amended) The processor readable storage medium of claim 29, wherein ~~the step of~~ modeling a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design;

determining whether the lookup table comprises a first entry that contains the plurality of read

address bits in an address field and a valid bit of the first entry is asserted; and

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and the valid bit of the first entry is asserted.

33. (currently amended) The processor readable storage medium of claim 32, wherein ~~the step of~~ modeling a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and the valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

34. (currently amended) An apparatus for creating a memory model for use in modeling an electronic circuit design having a physical memory, the apparatus comprising:

an output device;

a processor, in communication with the output device; and

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:

~~receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;~~

~~receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;~~

~~receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;~~

~~modeling a memory write operation of the electronic circuit design using a memory model;~~

~~modeling a memory read operation of the electronic circuit design using the memory model;~~

~~determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted;~~

~~determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted; and~~

accessing a description of the electronic circuit design;

replacing a portion of [[a]] the description of the electronic circuit design with the memory model, wherein the portion of the description relates to the physical memory, and wherein the memory model in the description represents the physical ~~memory.~~ memory, the memory model including a total number of entries that is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by:

determining a number of read ports of the physical memory,

determining a number of write ports of the physical memory,

computing a total number of memory operations that can be performed by the electronic circuit design per clock cycle based on the number of read ports and write ports, and

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles; and

simulating the electronic circuit design using the description, wherein simulating includes:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits,

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address,

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits,

modeling a memory write operation of the electronic circuit design using the memory model,

modeling a memory read operation of the electronic circuit design using the memory model,

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted, and

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.

35. (original) The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

36. (original) The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.

37. (original) The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

38. (original) The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

writing the plurality of write data bits to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

39. (original) The apparatus of claim 34, wherein the memory model comprises a lookup table.

40. (cancelled)

41. (currently amended) The apparatus of ~~claim 40~~ claim 34, wherein the code capable of programming the processor further ~~comprising~~ comprises the steps of:

determining a number of memory read operations in a property, the property being a set of behaviors of the physical memory; and

adding the number of memory read operations in a property to the total number of memory operations that can occur over the given number of clock cycles.

42. (currently amended) An apparatus for creating a model of an uninterpreted combinational block of an electronic circuit design using a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the apparatus comprising:

an output device;

a processor, in communication with the output device; and

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:

~~receiving the argument;~~

~~determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and~~

~~returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument; and~~

accessing a description of the electronic circuit design,

replacing a portion of [[a]] the description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combinational block, and wherein the lookup table in the description represents the uninterpreted combinational ~~block.~~ block, the lookup table including a total number of entries greater than or equal to a total number of times the uninterpreted combinational block will be evaluated over a given number of clock cycles, the total number of times the uninterpreted combinational block will be evaluated being computed by computing a total number of times the uninterpreted combinational block will be evaluated per clock cycle and multiplying the total number of times the uninterpreted combinational block will be modeled per clock cycle by the given number of clock cycles, and

simulating the electronic circuit design using the description, wherein simulating includes:

receiving the argument,

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted, and

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.

43. (original) The apparatus of claim 42, wherein the code capable of programming the processor further comprises the step of:

initializing the lookup table.

44. (original) The apparatus of claim 42, wherein the code capable of programming the processor further comprises the steps of writing the argument to an address field of a second entry having

an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.

45. (cancelled)

46. (currently amended) The method of claim 1, wherein the lookup table is a software data structure that is used to represent the physical memory and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

47. (currently amended) The method of claim 1, wherein the ~~lookup table is used to represent the physical memory with a~~ description of the electronic circuit design ~~by replacing a portion of~~ is a gate level description of the electronic circuit design ~~relating to the physical memory with the lookup table~~.

48. (previously presented) The method of claim 12, wherein the lookup table is a software data structure that is used to represent the uninterpreted combinational block and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

49. (currently amended) The method of ~~claim 14~~ claim 12, wherein the memory model is a software data structure that is used to represent the physical memory and the description of the electronic circuit design is a ~~hardware description language~~ gate level description of the electronic circuit design.

50. (cancelled)

51. (previously presented) The method of claim 29, wherein the lookup table is a

software data structure that is used to represent the physical memory and the description of the electronic design is a hardware description language description of the electronic circuit design.

52. (new) The method of claim 1, wherein simulating the electronic circuit design includes:

verifying operation of the electronic circuit design using a set of properties.

53. (new) The method of claim 12, wherein simulating the electronic circuit design includes:

verifying operation of the electronic circuit design using a set of properties.

54. (new) The method of claim 14, wherein simulating the electronic circuit design includes:

verifying operation of the electronic circuit design using a set of properties.

55. (new) The processor readable storage medium of claim 29, wherein simulating the electronic circuit design includes:

verifying operation of the electronic circuit design using a set of properties.

56. (new) The apparatus of claim 34, wherein the step of simulating the electronic circuit design includes:

verifying operation of the electronic circuit design using a set of properties.

57. (new) The apparatus of claim 42, wherein the step of simulating the electronic circuit design includes:

verifying operation of the electronic circuit design using a set of properties.